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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/035,607	12/28/2001	Peter F. Corbett	112056-0031	3778

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 09/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/035,607	CORBETT ET AL.	
	Examiner	Art Unit	
	James C Kerveros	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/5,3/12,3/25,02*, 3/28/03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-41 are pending and are hereby presented for examination, in response to the present Application filed 12/28/2001.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Han et al. (US 6158017).

Regarding independent Claim 1, Han discloses a method and apparatus for storing parity and rebuilding the data contents of two failed disks in a storage array, comprising the steps of: Providing the storage array, which is defined as a matrix (DH2), with a number of storage devices N+1 disks (d0-d7) each logically divided into N-1 data blocks, where N is a prime number, shown in (FIGS. 2, 4 and 8 to 10). The predetermined number of storage devices n is p+1, wherein n=p+1 and p is a prime number. FIG. 4 shows a disk array including six disks (N+1=6) d0 to d5, where p is a prime number N. If N=5, then (5+1=6), which is the predetermined number of storage devices "n".

Including a plurality of first devices configured to store data and row parity, and diagonal parity device configured to store diagonal parity, such as data blocks of a row being defined as a horizontal parity group and upwardly continuous diagonal line being defined as a diagonal parity group. Defining the data blocks of the last disk as the horizontal parity blocks. Defining the data blocks existing in the (N-1) row of the matrix as the diagonal parity blocks. Analyzing a diagonal parity group including one of error data blocks of the two failed disks to restore the one error data block, and the horizontal parity group including the restored one error data block to restore another error data block, where the analyzing step is repeated to completely rebuilt the data contents of the two failed disks (Abstract and Summary of the Invention).

A plurality of first devices [d0 to d5] configured to store data and row parity, FIG. 4, which shows a disk array including six disks (N+1=6) d0 to d5, each of which is logically divided into four blocks (N-1=4), where (30) represents the horizontal parity group including the second block b1. The hatched blocks of the sixth disk d5 represent the horizontal parity blocks. FIG. 8 shows the horizontal parity group Nos. 0, 1, 2, 3, and 4 of the DH2 parity arrangement in the case of N=7, where the hatched blocks H0 to H4 represent the horizontal parity blocks of the horizontal parity groups.

One diagonal parity device configured to store diagonal parity, defined in the Definition 3 and shown in FIG. 4. The blocks enclosed in the slotted line (32) represent the second parity group. In addition, the blocks of the fourth row (i=3) marked with dots represent the diagonal parity blocks to respectively store the parity values of the

diagonal parity groups. FIG. 9 illustrates the diagonal parity groups N=7, where the blocks D0 to D6 marked with dots represent the diagonal parity blocks.

Regarding independent Claims 7, 18, 24, 30, 36, 41, in addition to the common limitations as applied to claim 1, above, Han discloses a processing element controller 4 (see FIG. 2) configured to execute the storage operating system to thereby invoke storage access operations to and from the array in accordance with the R-D parity technique. "The parity storage algorithm of the DH2 parity arrangement provides a method for obtaining the parity values of the data blocks of the parity groups by XOR'ing, as shown in FIG. 15. A disk array of (N+1) is controlled by the controller 4 (see FIG. 2) to store the horizontal and diagonal parities respectively through steps 210 and 220".

Regarding independent Claims 1, 7, 18, 24, 30, 36, 41, Han does not disclose the feature of "one diagonal parity device configured to store diagonal parity". In FIG. 10, Han depicts the parities and data in the form of a matrix of N=7 of the DH2 parity arrangement, where H0 to H4 represent the horizontal parity blocks of the horizontal parity group Nos. 0 to 5, stored in the horizontal parity device N=7, while D0 to D6 represent the diagonal parity blocks of the diagonal parity group Nos. 0 to 6, stored in devices (d0-d6) disks. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to rearrange the matrix of Han by incorporating an additional dedicated disk for storing the diagonal parity group, since the matrix is expandable according to N+1 disks, where if N=7, then the number of disks is N+1=8. A person skilled in the art would have recognized that by adding a

dedicated disk, for storing diagonal parity, it provides redundancy and thus enchases system reliability.

Regarding Claims 2, 8, 19, 25, 31, Han discloses row parity blocks (H0 to H4) representing the horizontal parity blocks of the horizontal parity group Nos. (0 to 5), stored in the horizontal parity device N=7, FIG. 10.

Regarding Claims 3, 17, 23, 29, 33, 39, Han discloses first devices (d0-d6) including a plurality of data Devices (d0-d6), wherein the absent data devices are treated as containing zero-valued data, since they are not in the system.

Regarding Claims 4, 9, 20, 26, Han discloses computation of row parity blocks, which is replaced by a redundant encoding of data blocks. In FIG. 15, Han discloses a disk array, which is controlled by the controller 4 (see FIG. 2) to store the horizontal and diagonal parities respectively through steps 210 and 220. In step 210, the controller 4 calculates upon the horizontal parities of the horizontal parity group Nos. 0 to (N-3) to encode the horizontal parity blocks with the corresponding horizontal parities.

Regarding Claims 5, 13, 34, Han discloses a disk array (Structure of DH2 Parity Arrangement), which consists of N+1 disks where N=prime number, and each of the disks is logically divided into N-1 blocks, then a matrix is defined as an (N-1)*(N+1) matrix, table 3, where the total length of the devices is unequal, and wherein each row has one row parity block and one diagonal parity block, FIG. 4.

Regarding Claim 6, Han discloses a device, wherein locations of parity blocks shift from device to device within different stripes, FIG. 10.

Regarding Claims 15, 35, Han discloses, FIGS. 2 and 4, a device, wherein each sub-array (DISK) is organized as a distributed parity disk array (FIGS. 4 and 8 to 10).

Regarding Claims 10-12, 14, Han describes a storage operating system including a device storage layer configured as a RAID layer storage devices, wherein the storage devices are disks, such as "6 levels of disk arrays from 0 level to 5 level, classified according to structure and characteristics of the disk array. RAID is composed of a plurality of disks that provide large capacity, make it possible to parallel process to secure high performance, and employ the redundancy to rebuild the data contents of failed disks" cited in Patterson et al, "A Case for Redundant Arrays of Inexpensive Disks (RAID)", Chicago ACM SIGMOD Conf. Report, pp. 109-116, published in 1988, (Col. 1, lines 24-33, Han).

Furthermore, Han describes, "The parity arrangements of RAID level 6 have two group sizes because a data block requires two parity blocks. For example, 2D has horizontal and vertical parities, and EO, DH and DH2 have error correction groups of horizontal and diagonal parities. Representing group size G of the various parity arrangements, the names of the parity arrangements are indicated as a superscript of G, and the parity groups as a subscript of G. G without a subscript means take the average of two group sizes" (Table 8, Col. 18, lines 60-67, Han).

Regarding Claim 16, Han discloses devices, which are media adapted to store information contained within the data and parity blocks, as shown in FIG. 4, which illustrates diagonal and horizontal parity groups together with parity blocks according to the DH2 of FIG. 2.

Regarding Claims 21, 22, 27, 28, 37, 38, Han discloses means for dividing each device into blocks, means for organizing the blocks into stripes, and means for storing diagonal parity blocks on the diagonal parity disk for each of the diagonal parity sets of a stripe except one, such as "exclusive OR'ing (XORing) the contents of each of the horizontal and diagonal parity groups to obtain the parity value stored into the parity block of the corresponding horizontal or diagonal parity group", see Summary of the Invention. FIGS. 15, 16-18 illustrate a process of storing the parities according to the inventive DH2 arrangement with the number of disks N=7.

Regarding Claim 40, Han discloses predetermined number of storage devices n, wherein n=p+1 and p is a prime number. FIG. 4 shows a disk array including six disks (N+1=6) d0 to d5, where N is a prime number. If N=5, then n=(5+1=6), where "n" is the predetermined number of storage devices.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

4. Galbraith et al. (US 5537567) a parity block configuration in an array of storage devices with parity blocks confined to specific address ranges of each respective disk unit (rows of the array), each row containing multiple parity blocks. Each parity block represents the exclusive-OR of a stripe of data blocks located on a diagonal of the array.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
Email: james.kerveros@uspto.gov

Date: 23 August 2004
Office Action: Non-Final Rejection

By: _____

James C Kerveros
Examiner
Art Unit 2133

ALBERT DECADY
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